Agilent Technologies
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Surface Mount PIN Diodes

Technical Data

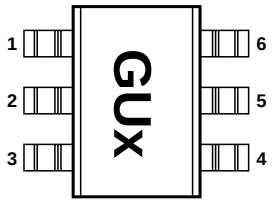
HSMP-386x Series

Features

- **Unique Configurations in Surface Mount Packages**
  - Add Flexibility
  - Save Board Space
  - Reduce Cost
- **Switching**
  - Low Distortion Switching
  - Low Capacitance
- **Attenuating**
  - Low Current Attenuating for Less Power Consumption
- **Matched Diodes for Consistent Performance**
- **Better Thermal Conductivity for Higher Power Dissipation**
- **Low Failure in Time (FIT) Rate[1]**

Note:
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Pin Connections and Package Marking, SOT-363



Notes:
1. Package marking provides orientation, identification, and date code.
2. See "Electrical Specifications" for appropriate package marking.

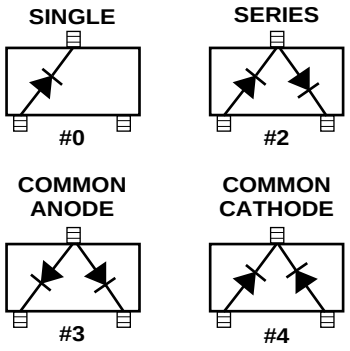
Description/Applications

The HSMP-386x series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low capacitance is the driving issue for the designer.

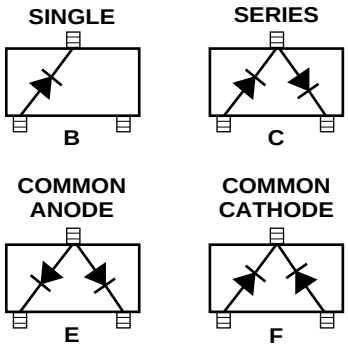
The HSMP-386x series Total Capacitance (C_T) and Total Resistance (R_T) are typical specifications. For applications that require guaranteed performance, the general purpose HSMP-383x series is recommended.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

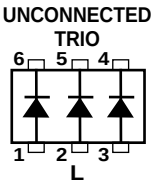
Package Lead Code Identification, SOT-23 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Package Lead Code Identification, SOT-363 (Top View)



Absolute Maximum Ratings[1] T_C = +25°C

Symbol	Parameter	Unit	SOT-23	SOT-323
I_f	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	50	50
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Electrical Specifications T_C = 25°C, each diode

PIN General Purpose Diodes, Typical Specifications T_A = 25°C

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Typical Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)
3860	F0[1]	0	Single	50	3.0/1.5*	0.20
3862	F2[1]	2	Series			
3863	F3[1]	3	Common Anode			
3864	F4[1]	4	Common Cathode			
386B	L0[2]	B	Single			
386C	L2[2]	C	Series			
386E	L3[2]	E	Common Anode			
386F	L4[2]	F	Common Cathode			
386L	LL[2]	L	Unconnected Trio			
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 10 mA f = 100 MHz I_F = 100 mA*	V_R = 50 V f = 1 MHz

Notes:
1. Package marking code is white.
2. Package marking code is laser marked.

HSMP-386x Typical Parameters at T_C = 25°C

Part Number HSMP-	Total Resistance R_T (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
386x	22	500	80	0.20
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA T_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	V_R = 50 V f = 1 MHz

Typical Performance, T_C = 25°C, each diode

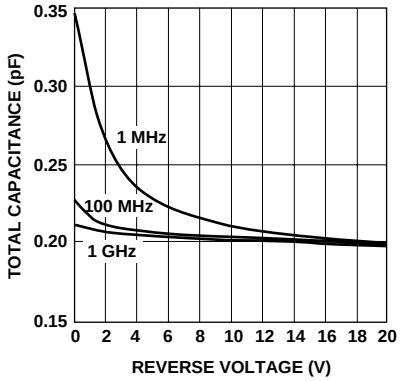


Figure 1. RF Capacitance vs. Reverse Bias.

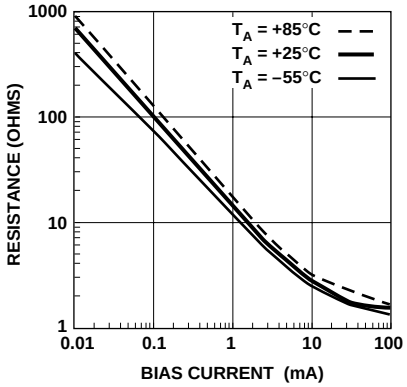


Figure 2. Typical RF Resistance vs. Forward Bias Current.

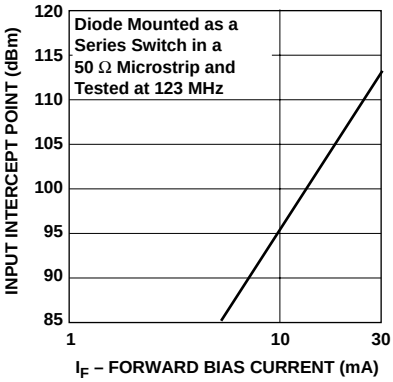


Figure 3. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

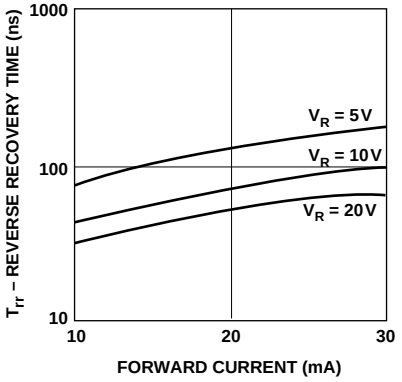


Figure 4. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages.

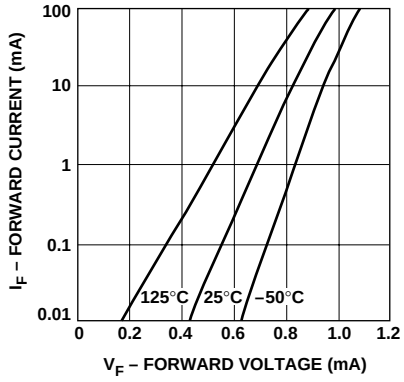
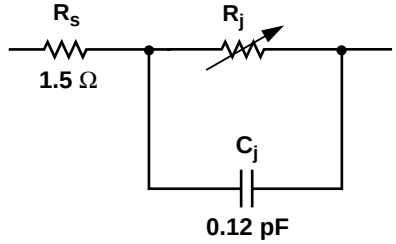


Figure 5. Forward Current vs. Forward Voltage.

Equivalent Circuit Model

HSMP-386x Chip*



$R_T = 1.5 + R_j$

$C_T = C_P + C_j$

$R_j = \frac{12}{I^{0.9}}\ \Omega$

I = Forward Bias Current in mA

* See AN1124 for package models

Typical Applications for Multiple Diode Products

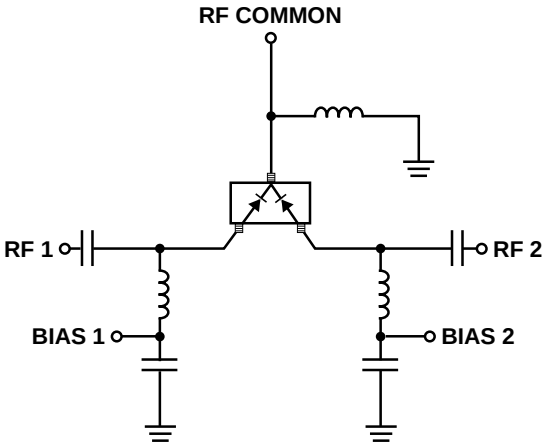


Figure 6. Simple SPDT Switch, Using Only Positive Current.

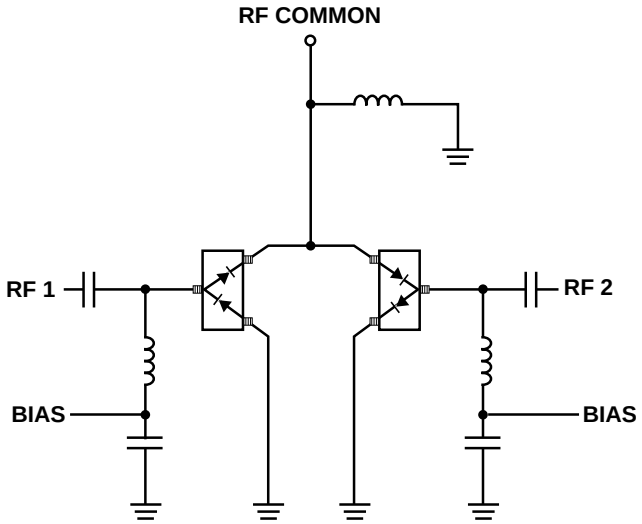


Figure 7. High Isolation SPDT Switch, Dual Bias.

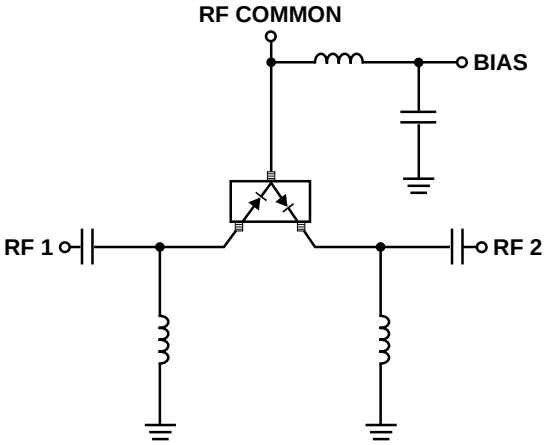


Figure 8. Switch Using Both Positive and Negative Current.

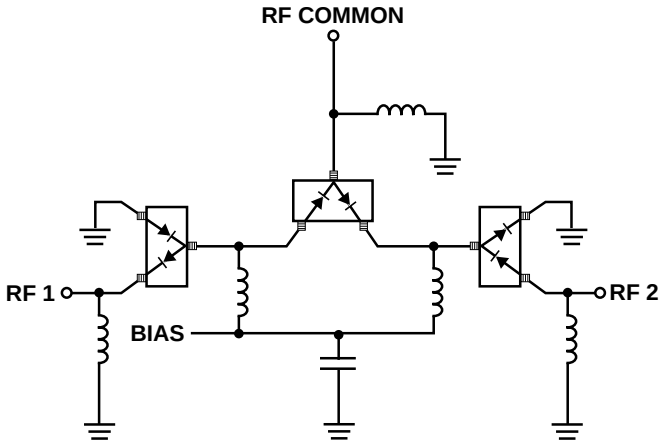


Figure 9. Very High Isolation SPDT Switch, Dual Bias.

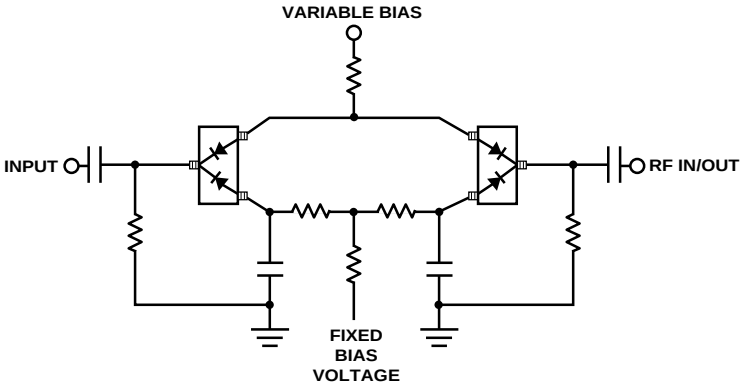


Figure 10. Four Diode π Attenuator. See AN1048 for details.

Typical Applications for Multiple Diode Products (continued)

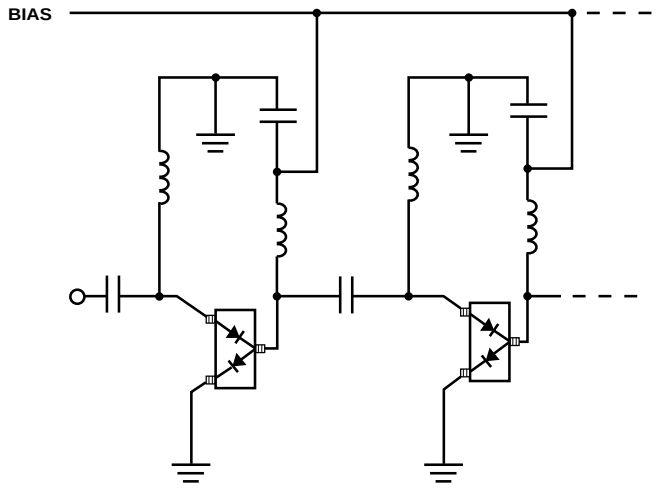


Figure 11. High Isolation SPST Switch (Repeat Cells as Required).

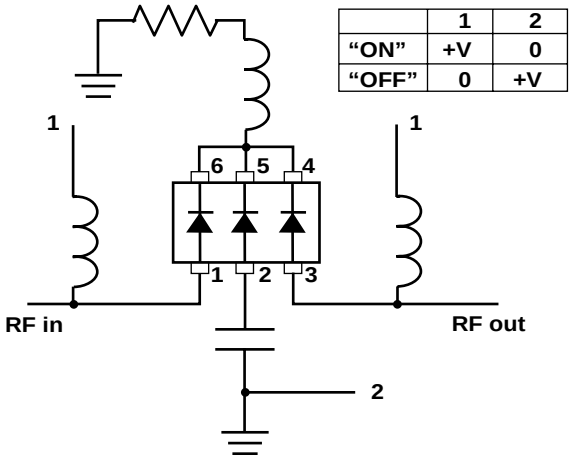


Figure 12. HSMP-386L Unconnected Trio used in a Positive Voltage, High Isolation Switch.

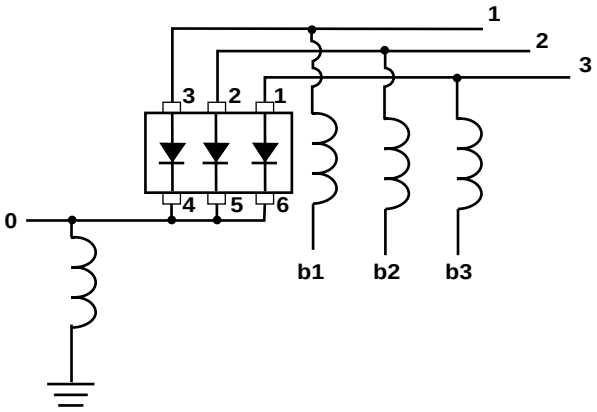


Figure 13. HSMP-386L used in a SP3T Switch.

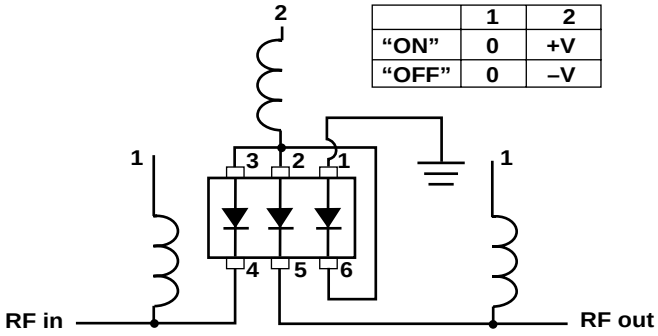


Figure 14. HSMP-386L Unconnected Trio used in a Dual Voltage, High Isolation Switch.

Ordering Information

Specify part number followed by option. For example:

HSMP - 386x - XXX

- XXX: Bulk or Tape and Reel Option
- 386x: Part Number; x = Lead Code
- HSMP: Surface Mount PIN

Option Descriptions

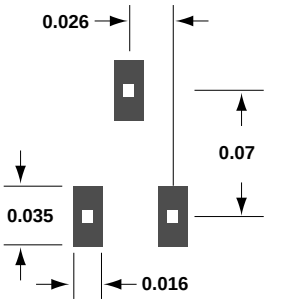
-BLK = Bulk, 100 pcs. per antistatic bag
-TR1 = Tape and Reel, 3000 devices per 7" reel
-TR2 = Tape and Reel, 10,000 devices per 13" reel

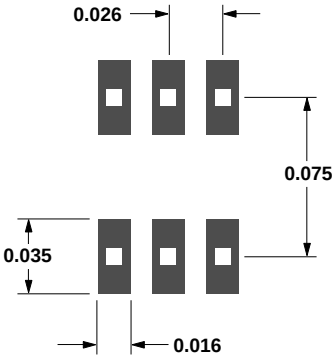
Tape and Reeling conforms to Electronic Industries RS-481, “Taping of Surface Mounted Components for Automated Placement.”

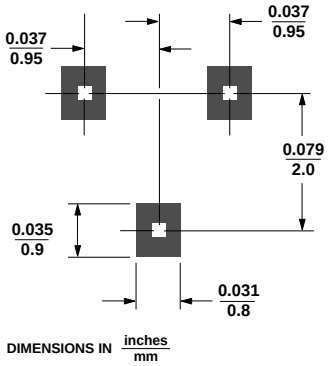
Assembly Information

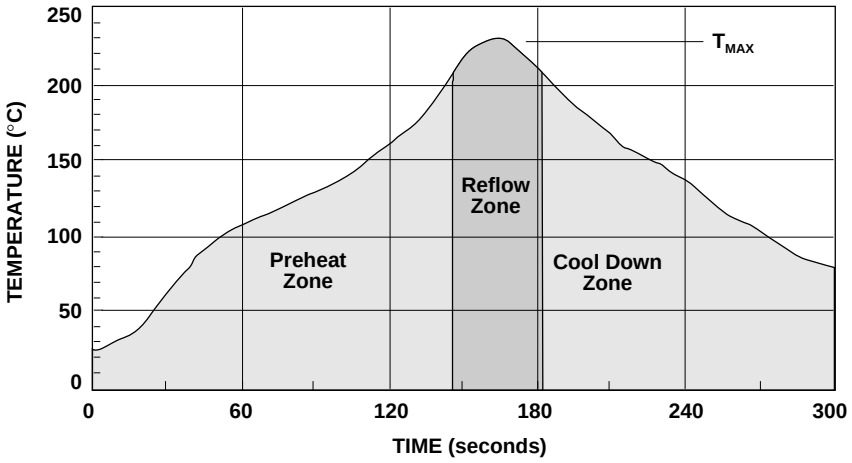
SOT-323 PCB Footprint

Recommended PCB pad layouts for the miniature SOT packages are shown in Figures 15, 16, 17. These layouts provide ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.



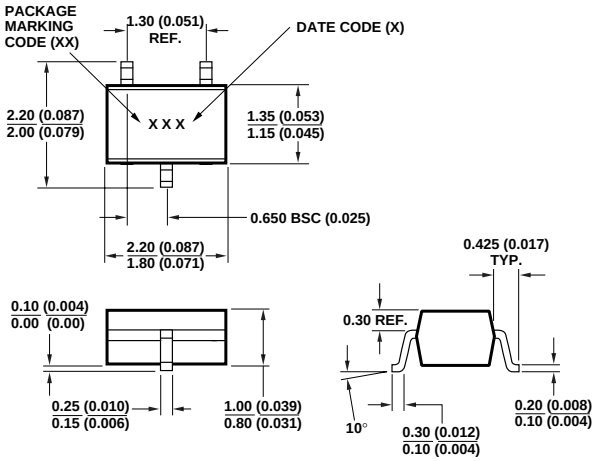






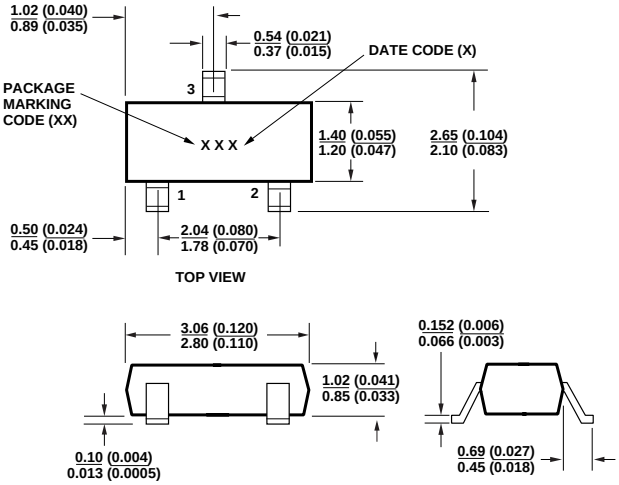
Package Dimensions

Outline SOT-323 (SC-70)



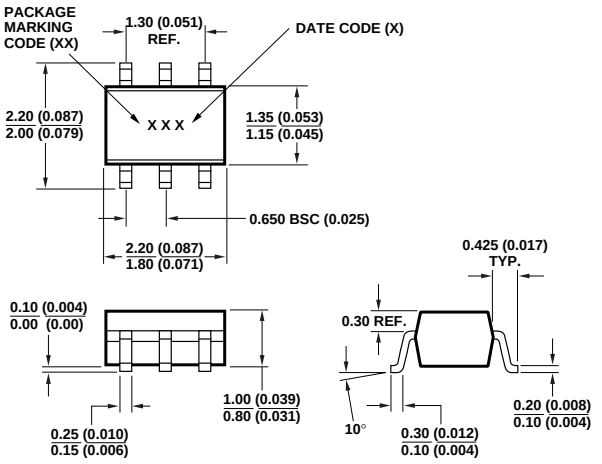
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 23 (SOT-23)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 363 (SC-70, 6 Lead)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package Characteristics

Lead Material ..... Copper (SOT-323/363); Alloy 42 (SOT-23)
Lead Finish ..... Tin-Lead 85-15%
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

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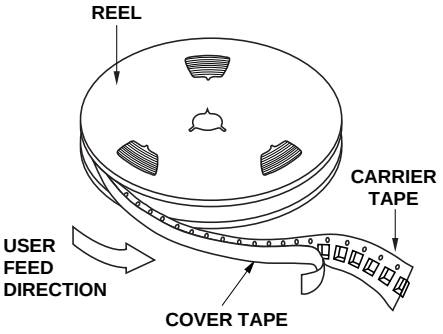
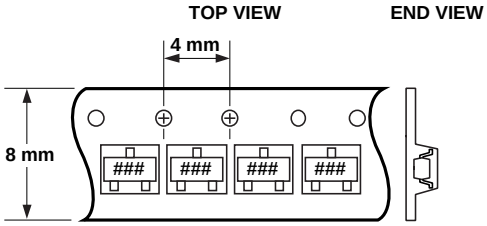
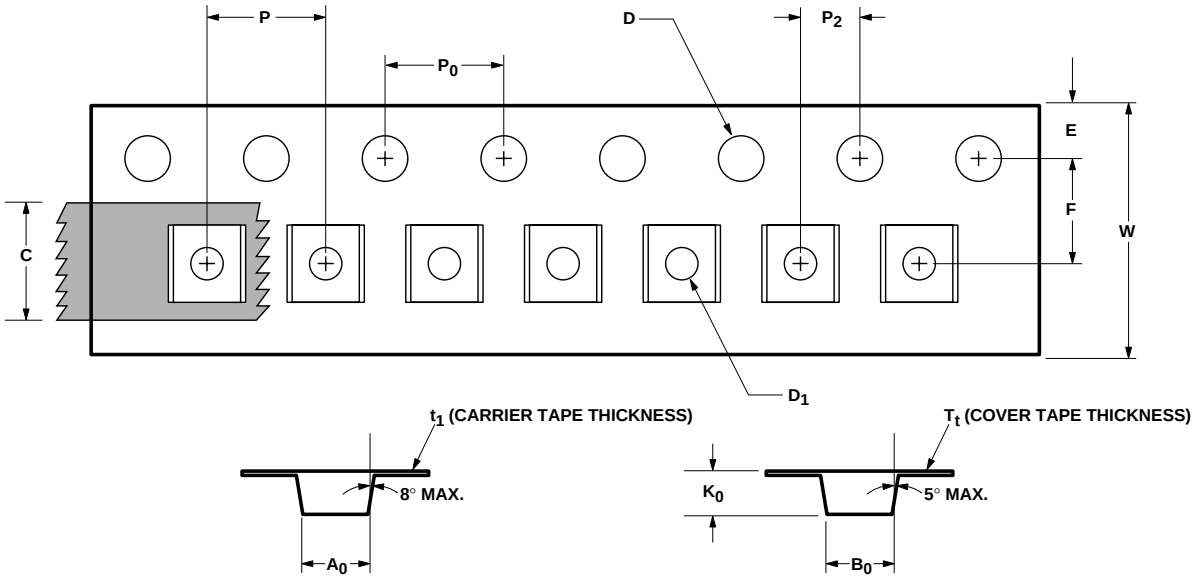
Device Orientation





Note: "###" represents Package Marking Code, Date Code.

Tape Dimensions
For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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