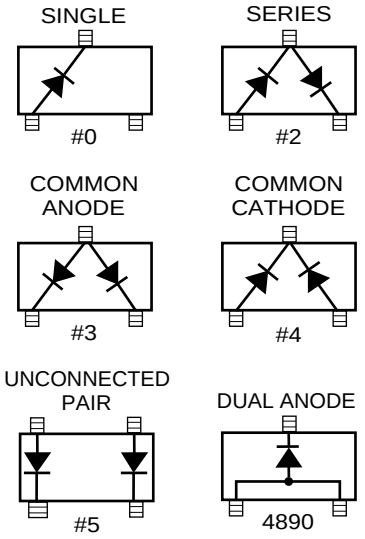
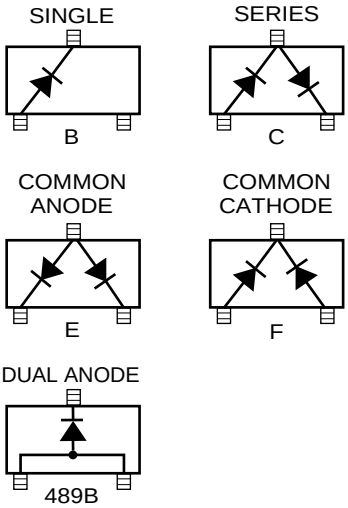
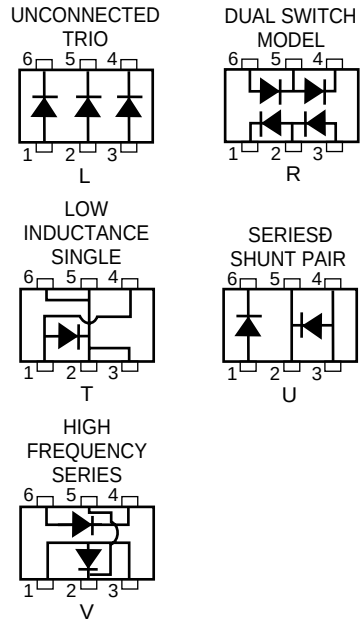
Package Lead Code Identification, SOT-23/143 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Package Lead Code Identification, SOT-363 (Top View)



Absolute Maximum Ratings [1] T_C = +25°C

Symbol	Parameter	Unit	SOT-23/143	SOT-323/363
I_f	Forward Current (1 ms Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	100	100
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
q_{jc}	Thermal Resistance [2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Electrical Specifications, T_C = 25°C, each diode

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3890	G0[1]	0	Single	100	2.5	0.30
3892	G2[1]	2	Series			
3893	G3[1]	3	Common Anode			
3894	G4[1]	4	Common Cathode			
3895	G5[1]	5	Unconnected Pair			
389B	G0[2]	B	Single			
389C	G2[2]	C	Series			
389E	G3[2]	E	Common Anode			
389F	G4[2]	F	Common Cathode			
389L	GL[2]	L	Unconnected Trio			
389R	S[2]	R	Dual Switch Mode			
389T	Z[2]	T	Low Inductance Single			
389U	GU[2]	U	Series-Shunt Pair			
389V	GV[2]	V	High Frequency Series Pair			
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	I_F = 5 mA f = 100 MHz	V_R = 5 V f = 1 MHz

Notes:
1. Package marking code is white.
2. Package is laser marked.

High Frequency (Low Inductance, 500 MHz – 3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code [1]	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)
489x	GA	Dual Anode	100	2.5	0.33	0.375	1.0
Test Conditions			$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	I_F = 5 mA	f = 1 MHz V_R = 5 V	V_R = 5 V f = 1 MHz	f = 500 MHz – 3 GHz

Note:
1. SOT-23 package marking code is white; SOT-323 is laser marked.

Typical Parameters at T_C = 25°C

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime t (ns)	Total Capacitance C_T (pF)
389x	3.8	200	0.20 @ 5 V
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 10 mA I_R = 6 mA	

HSMP-389x Series Typical Performance, T_C = 25°C, each diode

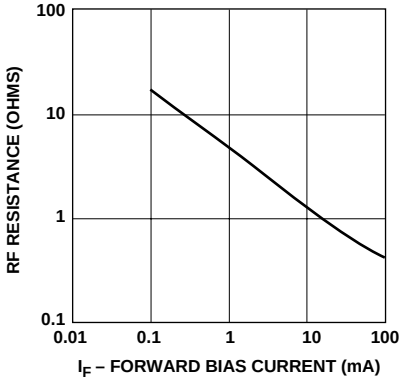


Figure 1. Total RF Resistance at 25°C vs. Forward Bias Current.

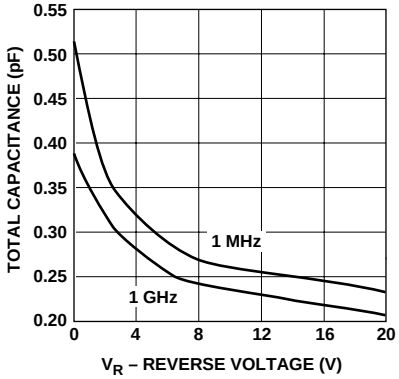


Figure 2. Capacitance vs. Reverse Voltage.

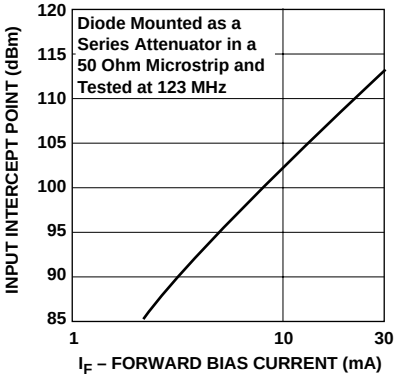


Figure 3. 2nd Harmonic Input Intercept Point vs. Forward Bias Current.

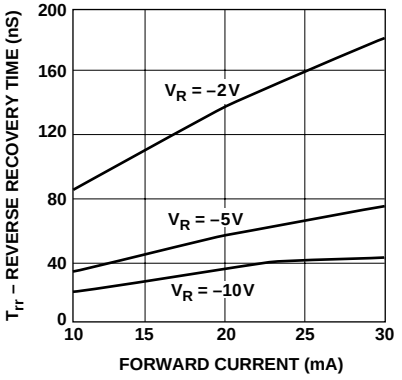


Figure 4. Typical Reverse Recovery Time vs. Reverse Voltage.

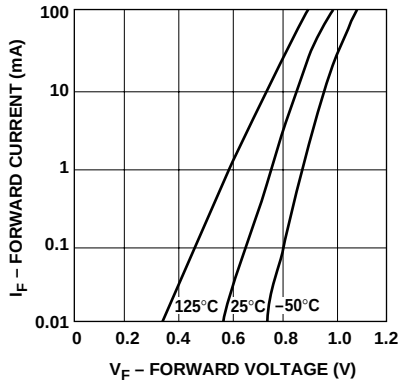


Figure 5. Forward Current vs. Forward Voltage.

Typical Applications for Multiple Diode Products

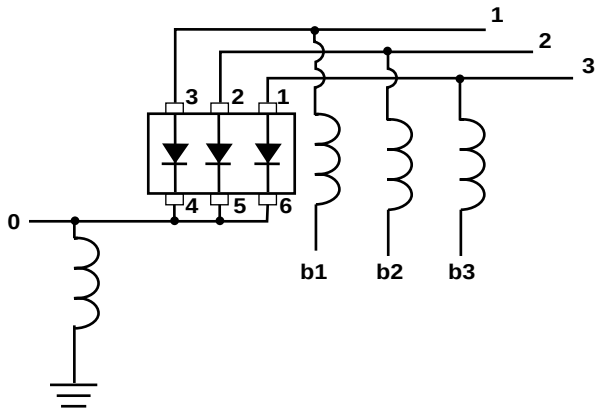
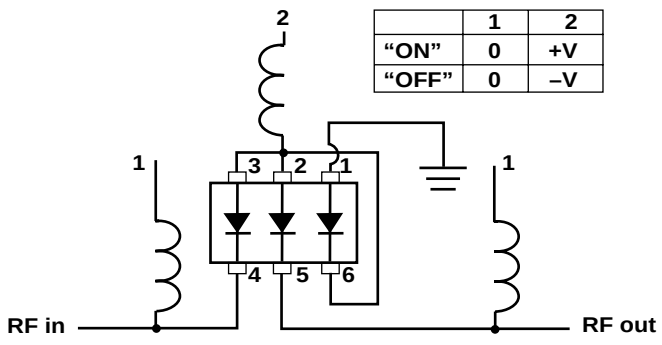


Figure 6. HSMP-389L used in a SP3T Switch.



	1	2
"ON"	0	+V
"OFF"	0	–V

Figure 7. HSMP-389L Unconnected Trio used in a Dual Voltage, High Isolation Switch.

Typical Applications for Multiple Diode Products (continued)

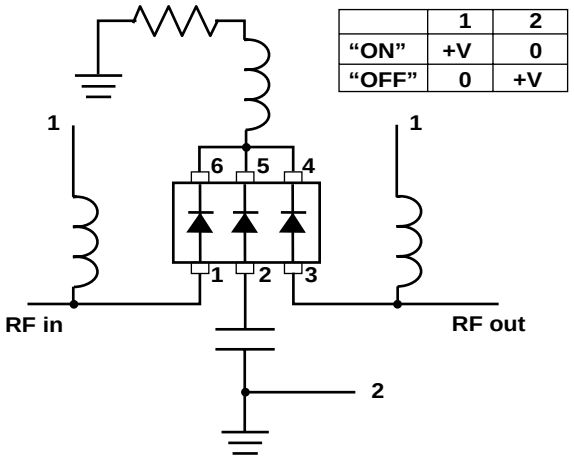


Figure 8. HSMP-389L Unconnected Trio used in a Positive Voltage, High Isolation Switch.

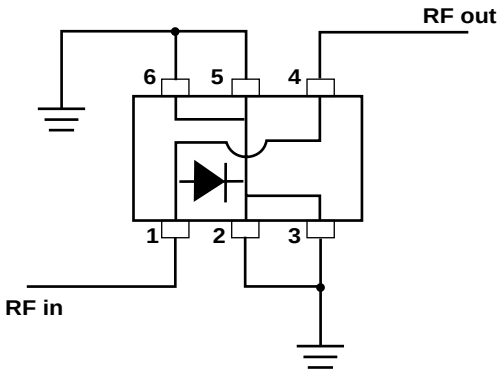


Figure 9. HSMP-389T used in a Low Inductance Shunt Mounted Switch.

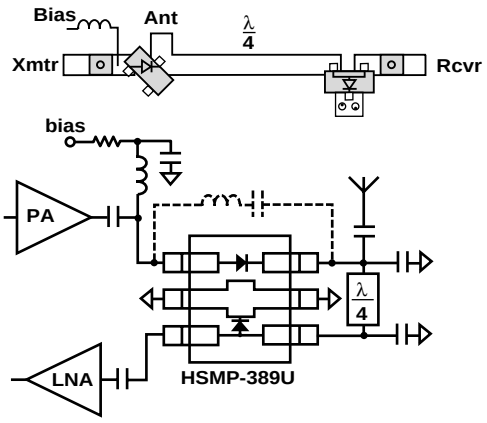


Figure 10. HSMP-389U Series/Shunt Pair used in a 900 MHz Transmit/Receive Switch.

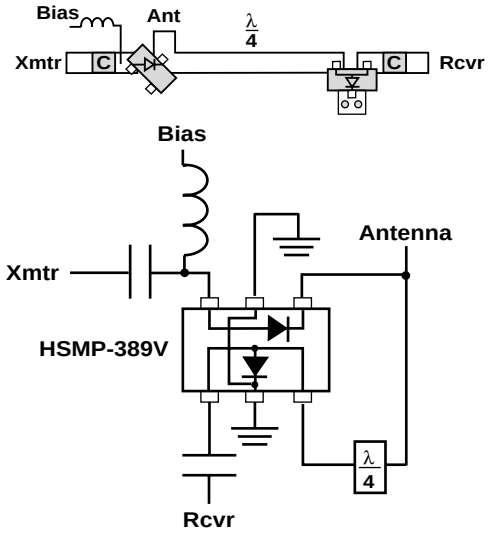


Figure 11. HSMP-389V Series/Shunt Pair used in a 1.8 GHz Transmit/Receive Switch.

Typical Applications for Multiple Diode Products (continued)

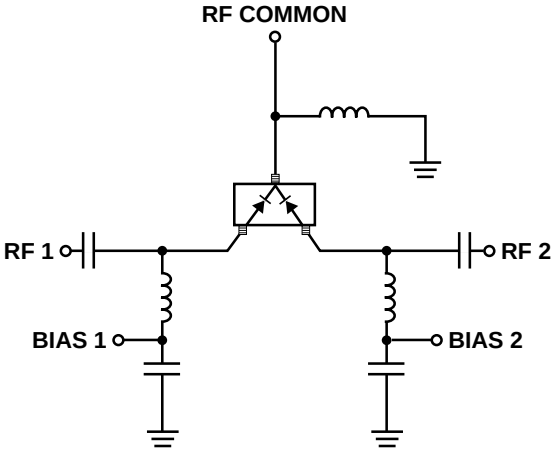


Figure 12. Simple SPDT Switch, Using Only Positive Current.

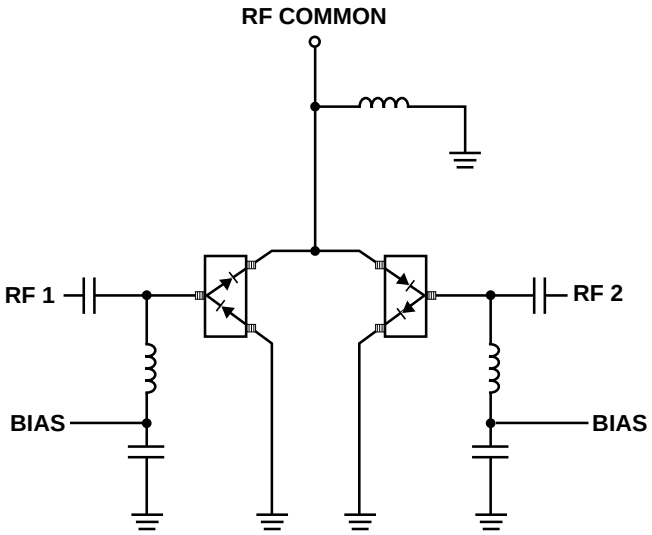


Figure 13. High Isolation SPDT Switch, Dual Bias.

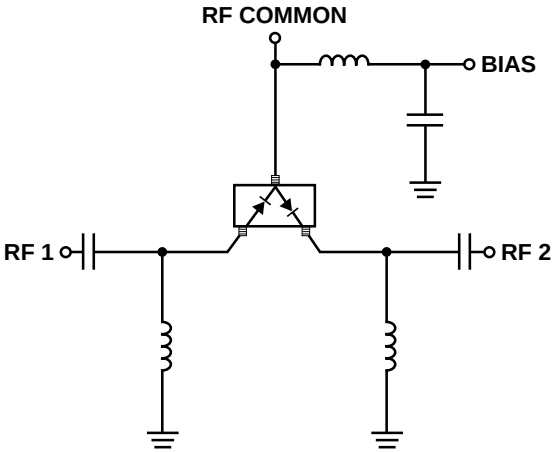


Figure 14. Switch Using Both Positive and Negative Bias Current.

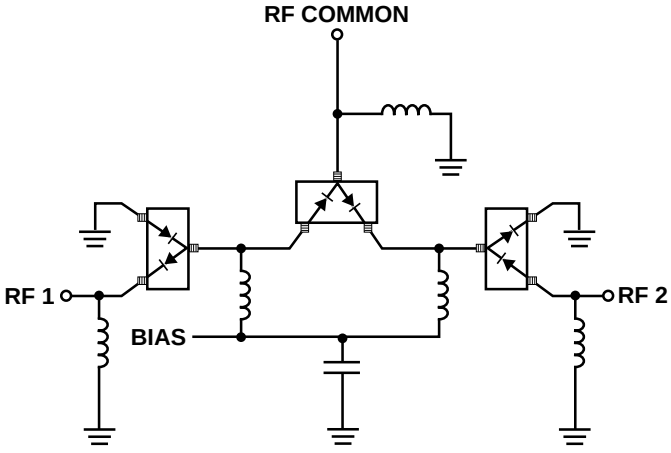
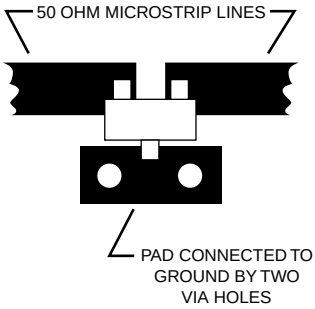
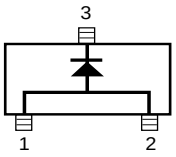
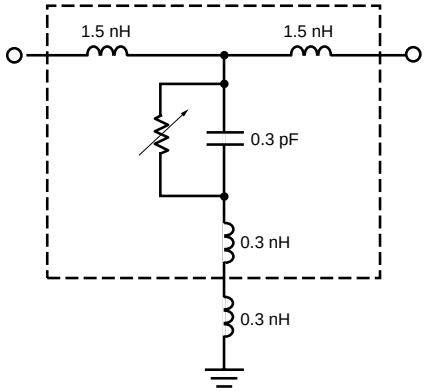


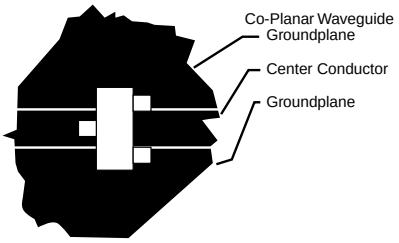
Figure 15. Very High Isolation SPDT Switch, Dual Bias.

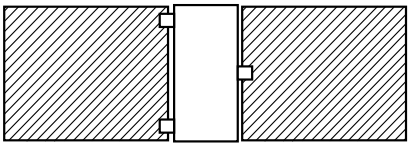


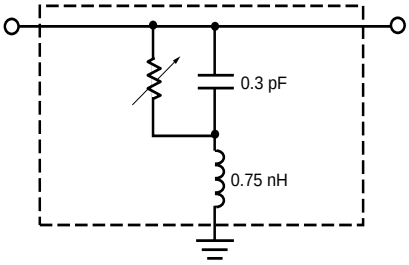


HSMP-489x



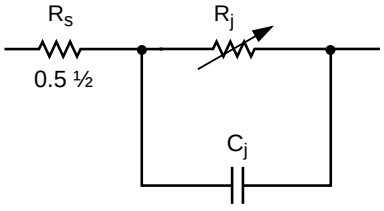






Equivalent Circuit Model

HSMP-389x Chip*



0.12 pF*

* Measured at -20 V

$R_T = 0.5 + R_j$

$C_T = C_P + C_j$

$R_j = \frac{20}{I^{0.9}}$ ½

I = Forward Bias Current in mA

* See AN1124 for package models

Assembly Information

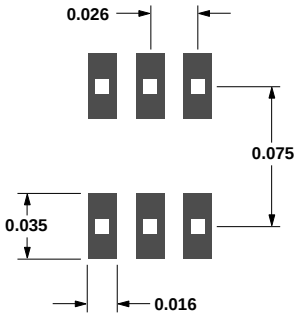


Figure 22. PCB Pad Layout, SOT-363. (dimensions in inches).

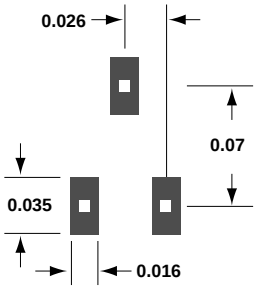


Figure 23. PCB Pad Layout, SOT-323. (dimensions in inches).

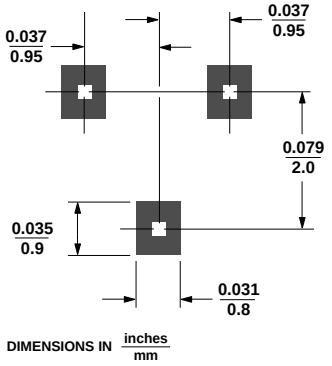


Figure 24. PCB Pad Layout, SOT-23.

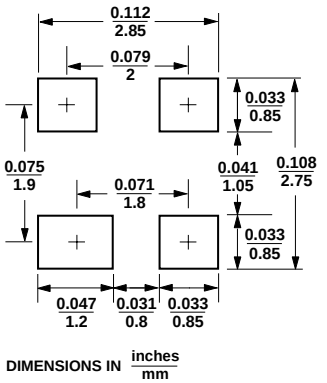


Figure 25. PCB Pad Layout, SOT-143.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT package, will reach solder reflow temperatures faster than those with a greater mass.

Agilent's diodes have been qualified to the time-temperature profile shown in Figure 26. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for Agilent diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

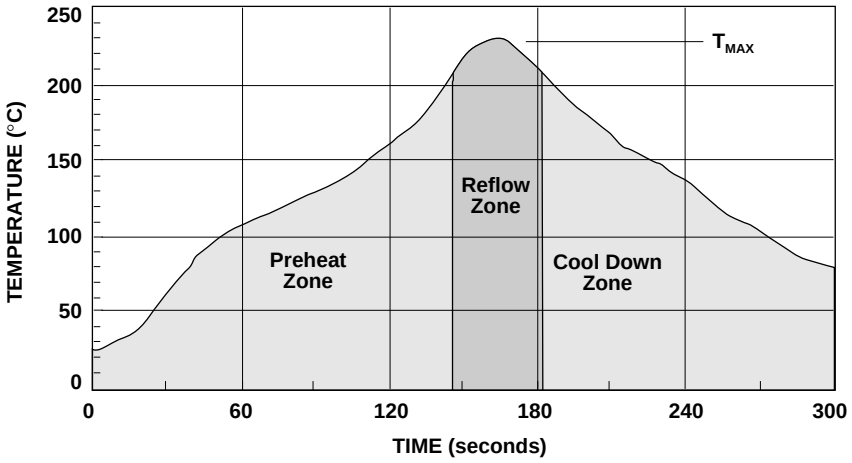
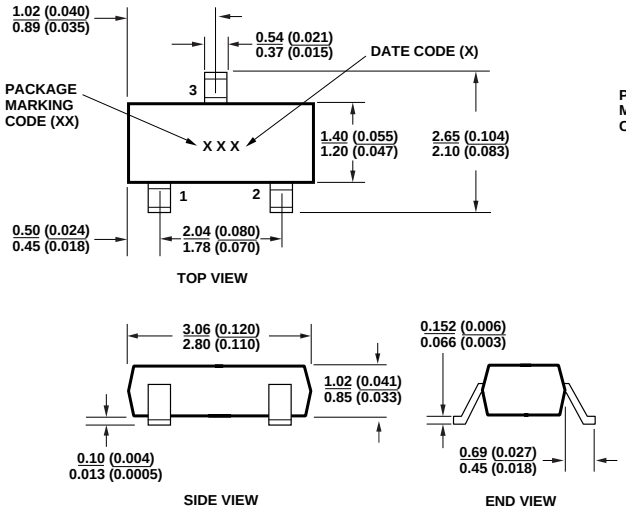


Figure 26. Surface Mount Assembly Profile.

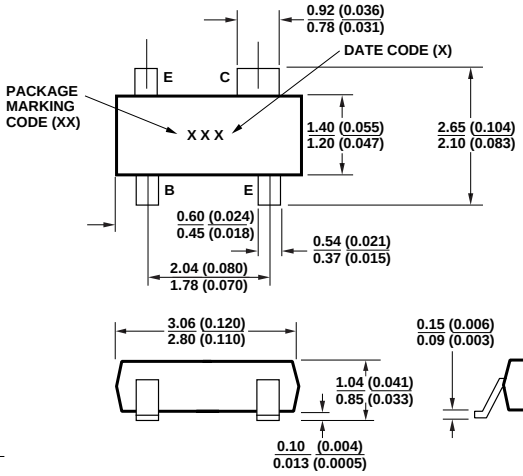
Package Dimensions

Outline 23 (SOT-23)



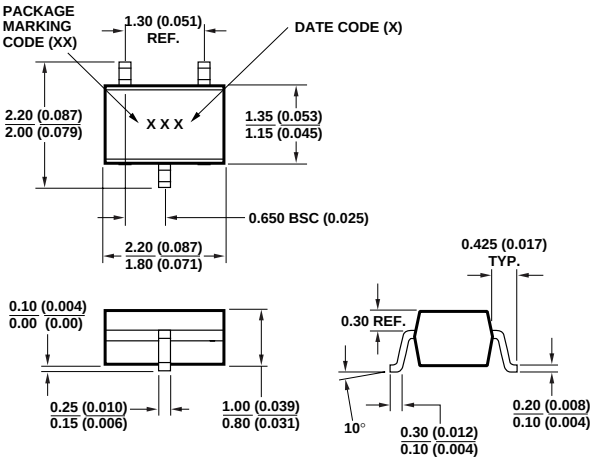
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)



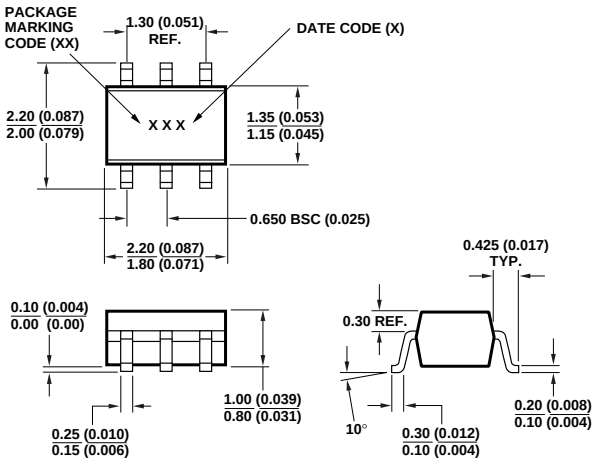
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline SOT-323 (SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 363 (SC-70, 6 Lead)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package Characteristics

Lead Material ..... Copper (SOT-323/363); Alloy 42 (SOT-23/143)
Lead Finish ..... Tin-Lead 85-15%
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Ordering Information

Specify part number followed by option. For example:

HSMP - 389x - XXX

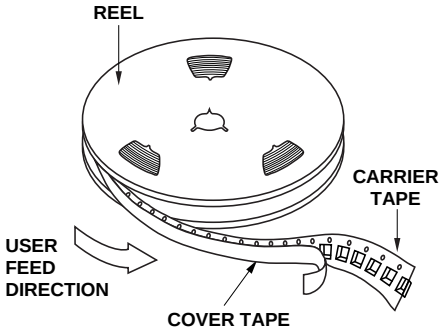
- XXX — Bulk or Tape and Reel Option
- 389x — Part Number; x = Lead Code
- HSMP — Surface Mount PIN

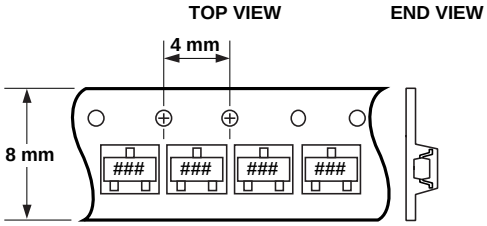
Option Descriptions

-BLK = Bulk, 100 pcs. per antistatic bag
-TR1 = Tape and Reel, 3000 devices per 7" reel
-TR2 = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, “Taping of Surface Mounted Components for Automated Placement.”

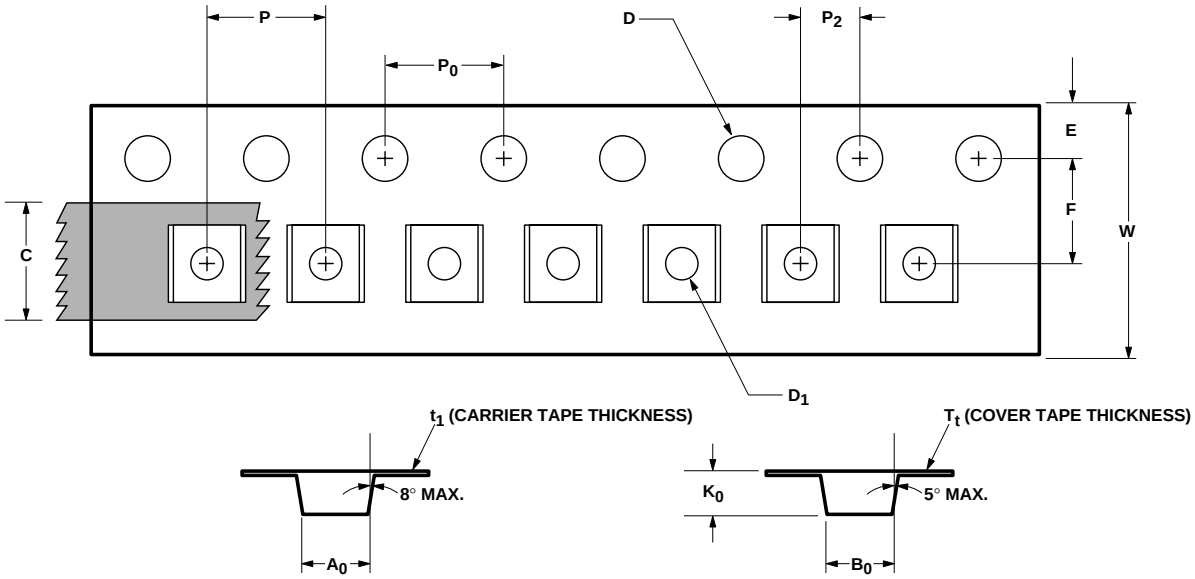
Device Orientation





Note: "###" represents Package Marking Code, Date Code.

Tape Dimensions
For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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